CLAIM AMENDMENTS

Claims 1-7 (Cancelled)

8. (Currently Amended) A semiconductor device TSOP (Thin Small Outline~~)~~ Package) having:

upper and lower semiconductor chips arranged between a first lead portion and a second lead portion, respectively, on two opposing sides of said semiconductor device, in plan view;

a first die pad integrated with and not coplanar with said first lead portion and located on one side of a reference plane passing through a central position between a first surface and a second surface of said first and second lead portions; and

a second die pad integrated with and not coplanar with said second lead portion and located on a second side of the reference plane, wherein said lower semiconductor chip is supported by said first die pad ~~and~~, said upper semiconductor chip is supported by said second die pad ~~portion~~, and said upper and lower semiconductor chips are partially overlapping and overlap in height ~~with~~ said first and second lead portions.

9. (Previously Presented) The semiconductor device according to claim 8, including:

a first lead frame connected to said first die pad and located, with said first lead portion, on the first side of said reference plane, and

a second lead frame connected to said first die pad and located, with said second lead portion, on the second side of said reference plane.

10. (Currently Amended) The semiconductor device according to claim 9, wherein

said first die pad ~~portion~~ is L-shaped and includes a first extension extending from an end of said first lead portion toward said second lead portion, and a first opposing portion continuing from said first extension and extending parallel to said first lead portion,

said second die pad ~~portion~~ is arranged, in plan view, opposite said first die pad , is L-shaped, and includes a second extension extending from an end of said second lead portion toward said first lead portion and a second opposing portion continuing from said second extension and extending parallel to said second lead portion,

said first extension and said first opposing portion have bottom surfaces supporting said lower semiconductor chip, and

said second extension and said second opposing portion have upper surfaces supporting said upper semiconductor chip.

11. (Previously Presented) The semiconductor device according to claim 8, wherein said first and second lead portions and said first and second die pads are integrated into a common lead frame, said reference plane passes centrally through the thickness of said lead frame, said first die pad supports said lower semiconductor chip of said partially overlapped upper and lower semiconductor chips, and said second die pad supports said upper semiconductor chip.

12. (Currently Amended) The semiconductor device according to claim 11, including adhesive layers respectively bonding said upper and lower semiconductor chips to said first and second die pads, wherein a center of the thickness of said first die pad ~~portion~~ and a center of the thickness of said second die pad ~~portion~~ are spaced from said reference plane in respective opposite directions, each by a distance equal to the sum of one-half the thickness of said lead frame and one-half the thickness of said adhesive layers bonding said upper and lower semiconductor chips to said first and second die pads.

Claims 13-15 (Cancelled).

16. (New) The semiconductor device according to claim 8, wherein said lower semiconductor chip is bonded to said first die pad and said upper semiconductor chip is bonded to said second die pad and including a first adhesive layer contacting both of said upper and lower semiconductor chips, and bonding said first die pad to said lower semiconductor chip, said second die pad to said upper semiconductor chip, and said lower semiconductor chip to said upper semiconductor chip.

17. (New) The semiconductor device according to claim 16 including wires electrically connecting said first lead portion to said upper semiconductor chip and connecting said second lead portion to said lower semiconductor chip.

18. (New) The semiconductor device according to claim 16, wherein said upper semiconductor chip is sandwiched by said first die pad and said first lead portion and said lower semiconductor chip is sandwiched by said second die pad and said second lead portion.